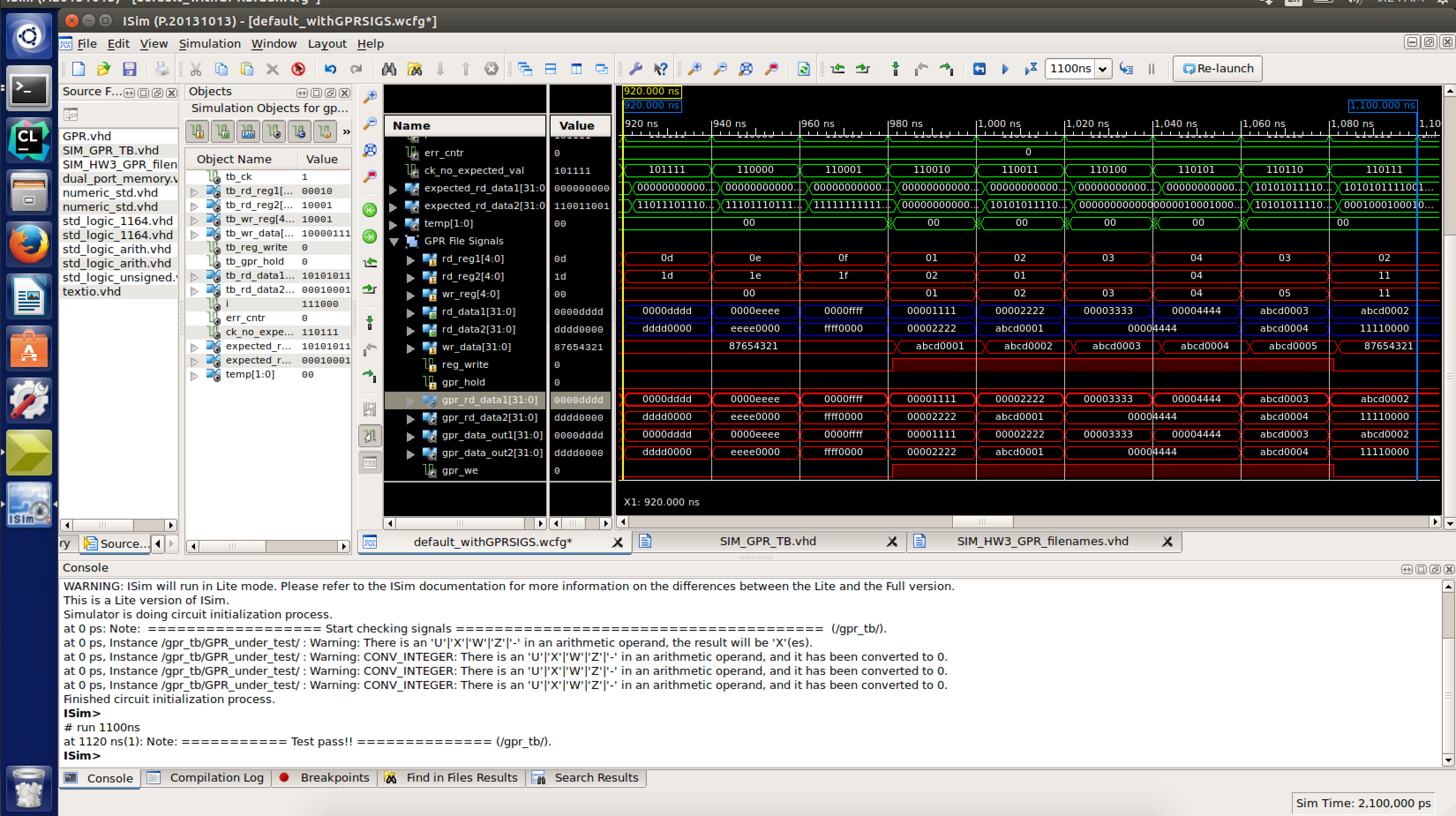
HW#3 GPR Simulation Report

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Simulation Screenshot



**RD\_DATA1 and RD\_DATA2 signal explanation**

Explanation about rd\_data1 and rd\_data2 signals during clock cycles 46-55:

CK GPR\_hold reg\_wr wr\_reg wr\_data rd\_reg1 rd\_reg1\_data rd\_reg2 rd\_reg2\_data

46 0 0 0 x"87654321" 12 x"0000CCCC" 28 x"CCCC0000"

47 0 0 0 x"87654321" 13 x"0000DDDD" 29 x"DDDD0000"

48 0 0 0 x"87654321" 14 x"0000EEEE" 30 x"EEEE0000"

49 0 0 0 x"87654321" 15 x"0000FFFF" 31 x"FFFF0000"

50 0 1 1 x"ABCD0001" 1 x"00001111" 2 x"00002222"

51 0 1 2 x"ABCD0002" 2 x"00002222" 1 x"ABCD0001"

52 0 1 3 x"ABCD0003" 3 x"00003333" 4 x"00004444"

53 0 1 4 x"ABCD0004" 4 x"00004444" 4 x"00004444"

54 0 1 5 x"ABCD0005" 3 x"ABCD0003" 4 x"ABCD0004"

55 0 0 17 x"87654321" 2 x"ABCD0002" 17 x"11110000"

The **rd\_data1** and **rd\_data2** signals reflect the signals “retrieved” from the registers as they are simulated by the TB during these cycles.   
During the simulation, since we use the program file “GPR\_TB\_Data.dat” to simulate the registers and signals – we can see the signals that were planted by the simulation. Meaning, these signals reflect what should have been retrieved during a real execution from the GPR registers.

In addition, our *beautiful* **coloring** reflects the writing of register data, and reading in the following clock cycles from the altered registers.